Physical ASIC Design Implementation Engineer

About the company

Qplox is a fast-growing company offering test and automation engineering. Headquartered in Leuven, with offices in Barcelona and Eindhoven.
Our clients are major multinational enterprises and local companies from automotive, semiconductors, RF, consumer electronics…. Our Test automation group offers a one stop shop for design of automated test benches, system integration production, lab automation and data acquisition systems, with a growing focus in IoT sensor networks.
Our consultancy department offers services in RF, semiconductors and electronics design and test, as well as on the crossing roads of Nanotechnology, Bio-Science Engineering and Biotechnology.

Job Description

We're looking for a Physical Implementation Engineer for full backend (P&R) projects from netlist-in to GDSII-out flow, for top level chips as well as block level blocks in technologies ranging from N5 to 180nm. This with the full understanding of the complete Cadence Innovus Place&Route flow.

The assignment

- Setup of full netlist In to GDSII-out P&R flow (libs, derating, lowpower,..)
- Place & Route: from floor planning until post route
- Solve setup/hold/SI/power/... violations
- Sign-off Timing and Physical/logical verification (LEC, DRC, LVS,...)
- Discuss constraints/specs with feedback results to and cooperate with customer.

Location: Leuven

Candidate Description

- 10 years of experience in physical implementation in advanced nodes (12 – 7nm) and hierarchical designs
- Debug capabilities
- Flexible work/project
- Good customer interaction
- tcl scripting
- You have an open mind and a fluent knowledge of English.
- You feel comfortable in a complex and demanding environment.
- Experience with Microsoft Office 365 tools, such as SharePoint, Teams, PowerApps, OneDrive,... is a must and with Azure DevOps an important plus.

We offer

An attractive salary package with extra benefits. A high tech, multicultural and young ambient. A fast track in a growing company. Formation in multidisciplinary environment plenty of learning opportunities.

Contact

Send your CV and application letter to jobs@qplox.com with the subject "**Physical ASIC Design Implementation Engineer".**