Digital Layout Backend Engineer

About the company

Qplox specializes in product qualification and release. We offer consultancy and engineering services for test and lab automation, characterization, verification, validation and end of line test. For a wide range of products, and with special focus in High tech.
Our engineering department develops custom made test and automation systems, electronic prototypes and test benches. Our consultancy department offers our clients a complete solution for their high tech qualification needs. From RF, Photonics, semiconductors… our engineers can help in the qualification of all your advanced products.

Job Description

You will be a member of the qplox R&D team, and working for our customer in the region of Leuven and part of our customer transceiver chip developments. Our customer is working on a complex mixed signal SOC in an advanced CMOS node. The successful candidate will work together with the Belgian implementation engineer assisting in the implementation and taking ownership of the power analysis and sign-off verification. He/she will set up the full power analysis and sign-off verification flow, execute on it, feed the information back to the other team members, analyze issues and assist in solving them.
The successful candidate needs to be a technical expert in the following areas covering the digital design flow :

- Writing, understanding and adapting SDC based timing constraints
- IR drop analysis
- Signal integrity (SI) analysis and closure
- Structured & hierarchical layout, manual placement and routing.
- power analysis (static and dynamic)
- DRC and LVS sign-off
- Clock tree synthesis (CTS): optimizing the clock tree is essential and often requires a mix of clock tree synthesis and (partial) manual instantiation of the clock tree for the most sensitive parts.
- Placement and routing
- static timing analysis (STA) and closure
- Logic synthesis: knowledge of physical synthesis is a big plus.

Candidate Description

- Strongly Desired Education and Experience:
- Minimum 8 years experience
- MS in EE, Computer Engineering, or equivalent field
- Experience with digital hardware: RTL design (VHDL, Verilog), logic optimization, RTL compiler, deep sub-micron.
- Experience with (mainly Cadence) backend tools: Innovus (CTS, CPF, SDC, STA, SI, …), Redhawk, ….
- Good communication skills
- Detail oriented and determined
- Team player

Key Words

RF transceivers, 2G, 3G, 4G, LTE, wireless technologies, mobile, Back End, RF IC, Layout, Cadence, CMOS.

We offer

Your performance and growth is monitored, assessed and rewarded, you will have an individual development plan based on your competences and interests. We offer an attractive salary package with extra-legal benefits. A high tech, multicultural

and young company with fast promotion and many learning possibilities in a growing, multidisciplinary company.

Contact

Send your CV to jobs@qplox.com or surf to www.qplox.com